LISTING OF CLAIMS

Claims 1-4. (Canceled)

Claim 5. (Currently Amended) A [The] memory device [of claim 3], comprising:

a substrate; and

a single transistor formed on the substrate, the transistor having a gate with a nonvolatile memory element, wherein the nonvolatile memory element is connected to first and second bit lines separated from each other, and wherein the first and second bit lines pass above the nonvolatile memory element.

Claims 6-17. (Canceled)

Claim 18. (Original) The memory device of claim 5, wherein the nonvolatile memory element includes:

semiconductor quantum dots formed on the gate insulating layer; and

an amorphous material layer covering the plurality of semiconductor quantum dots, wherein the amorphous material layer stores carriers emitted from the semiconductor quantum dots and maintains the carriers in a nonvolatile state until the emitted carriers are recaptured into the semiconductor quantum dots.

Claim 19. (Original) The memory device of claim 18, wherein the semiconductor quantum dots are silicon dots arranged at regular intervals.

Claim 20. (Original) The memory device of claim 18, wherein the amorphous material layer, which is an amorphous dielectric layer, is an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

Claims 21-23. (Canceled)

Claim 24. (Original) The memory device of claim 5, wherein a sense amplifier is connected to the first bit line as a current measuring means.

Claims 25-26. (Canceled)

Claim 27. (Currently Amended) A [The] semiconductor memory device [of claim 26], comprising:

a substrate;

a transistor formed on the substrate; and

a nonvolatile memory means formed between the transistor and the substrate and connected to first and second bit lines separated from each other, wherein the nonvolatile memory means includes an amorphous material layer formed on the substrate and semiconductor quantum dots formed on the amorphous material layer, wherein the amorphous material layer stores carriers emitted from the semiconductor quantum dots and maintains the carriers in a nonvolatile state until the emitted carriers are recaptured into the semiconductor quantum dots.

Claim 28. (Original) The semiconductor memory device of claim 27, wherein the transistor comprises:

first and second metal layer patterns formed on the amorphous material layer, both being separated from each other;

an insulating layer formed on the amorphous material layer so as to cover the semiconductor quantum dots and the first and second metal layers;

and a word line formed on the insulating layer at a position corresponding to a position where the semiconductor quantum dots are formed.

Claim 29. (Original) The semiconductor memory device of claim 27, wherein the semiconductor quantum dots are a plurality of spaced silicon dots.

Claim 30. (Original) The semiconductor memory device of claim 27, wherein the amorphous material layer, which is an amorphous dielectric layer, is an amorphous silicon nitride layer, an amorphous alumina layer or a silicon oxide layer (SiO_2).

Claim 31. (Original) The semiconductor memory device of claim 28, wherein the semiconductor quantum dots are a plurality of spaced silicon dots.

Claim 32. (Original) The semiconductor memory device of claim 28, further comprising:

an interlayer dielectric layer formed on the insulating layer for covering the word line;

a via hole formed in the interlayer dielectric layer and the insulating layer so that the first metal pattern is exposed; and

a fourth metal layer pattern formed on the interlayer dielectric layer for filling the via hole and passing across the word line.

33-64. (Canceled)